# PFC-PWM CONTROLLER HAVING INTERLEAVED SWITCHING

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

[0001] The present invention generally relates to the field of switching mode power converters. More particularly, the present invention relates to PFC-PWM controllers.

### 2. Description of the Prior Art

[0002] The purpose of Power Factor Correction (PFC) is to correct ~~the~~a line current of a power supply. Power Factor Correction produces a sinusoidal input current waveform that is in phase with ~~the~~a line input voltage. With a PFC circuitry in ~~the~~a front-end of the power supply, a DC-to-DC ~~power~~ converter can significantly reduce ~~the~~ ~~magnitude of~~ power loss and heat dissipation in ~~the~~ power contribution ~~system~~ systems.

Recently enacted environmental regulations in the U.S. and in Europe not only require most consumer products to have built-in PFC function, but ~~they~~ also strictly limit overall power consumption. Specifically, the amount of power consumption permitted for supervising and remote control purposes has been significantly reduced. Therefore, reducing power consumption under standby mode becomes a major concern among electronics manufacturers.

[0003] Traditional DC-to-DC ~~power~~ converters with PFC function still have high power consumption under light-load and zero-load conditions. Because of this, many present-day electronic product designs are not compliant with power conservation

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requirements. Furthermore, when a the PFC ~~circuit~~ circuitry is cascaded with PWM (pulse width modulation) circuitry, significant switching interference and EMI (electrical-magnetic interference) ~~can~~ could occur. To alleviate these problems, most DC-to-DC ~~power~~ converters incorporate a PWM ~~circuit~~ circuitry having some form of synchronous switching.

[0004] One method of synchronizing PFC and PWM signals is described in U.S. Patent No. 5,565,761 (Hwang). Hwang discloses a leading-edge and trailing-edge modulation technique, in which the PFC boost converter switches (the first stage) and the DC-to-DC power converter switches (the second stage) are turned on and off at the same time. This minimizes the duration of the temporary zero-load period and reduces the magnitude of the ripple voltage delivered to the load.

[0005] However, one drawback of Hwang's invention is that power consumption is not reduced under light-load and zero-load conditions. Another drawback of Hwang's invention is poor output response to dynamic loads because of the duty cycle of the second stage being not directly controlled by the output voltage.

[0006] Furthermore, Hwang's invention teaches a DC-to-DC power converter having a dc ok comparator coupled to the first stage. The dc ok comparator prevents the second stage from turning on if the output voltage of the first stage is below a threshold value. However, the dc ok comparator is sensitive to noise interference. Spike and overshoot signals can incorrectly turn on the second stage.

[0007] Another drawback of Hwang's invention is that it generates significant noise and EMI during leading edge and trailing edge switching. To minimize ripple voltage, the PFC boost converter switches and the DC-to-DC converter switches are turned on and off at the same time. However, this technique mutually modulates the switching noise, and doubles its magnitude. Furthermore, the PFC-PWM controller according to Hwang simultaneously conducts the parasitic devices of the PFC and

PWM stages. This can result in the creation of a multi-resonant tank that generates substantial high frequency noise.

[0008] The objective of the present invention is to provide a PFC-PWM controller that overcomes the drawbacks of the prior art. The present invention also includes a means for reducing power consumption while the power converter is operating in standby mode.

SUMMARY OF THE INVENTION

[0009] The present invention provides a PFC-PWM controller having interleaved switching. The PFC-PWM controller includes a PFC stage, a PWM stage, a sequencer, a power manager and an oscillator. The PFC stage is used for generating a PFC signal in response to the a line voltage and a first feedback voltage. The PFC signal is used to control switches of the a PFC boost converter switches of a power converter. The PWM stage generates a PWM signal in response to a second feedback voltage. The PWM signal controls switches of the a DC-to-DC power converter switches of the power converter.

[0010] The first feedback voltage is derived from the a PFC boost converter feedback loop. The second feedback voltage is derived from the a DC-to-DC power converter feedback loop. The magnitudes of these feedback voltages are proportional to the a load of the power converter. Conversely, these two the first and second feedback voltages are inversely proportional to the magnitude of the an output voltage of the power converter.

[0011] The PFC-PWM controller includes a the power manager to generate a discharge current and a burst-signal. Under light-load conditions, the magnitude of the discharge current is in proportion proportional to both the first feedback voltage and the

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second feedback voltage. When a low-load condition is sustained longer than a first delay-time, this achieves a suspended condition. The burst-signal is generated to disable the PFC signal while the power-supply converter is in the suspended condition.

[0012] The PFC-PWM controller includes an the oscillator for generating a ramp-signal, a slope-signal and a pulse-signal. The ramp-signal and the slope-signal are synchronized with the pulse-signal, such that the pulse-signal is inserted in between the PFC signal and the PWM signal. The A rising-edge of the pulse-signal disables the PFC signal. The A falling-edge of the pulse-signal enables the PWM signal. The A pulse width of the pulse-signal is increased in response to decreases a decrement of the discharge current. The first feedback voltage is compared with the slope-signal to generate the PFC signal, and the second feedback voltage is compared with the ramp-signal to generate the PWM signal.

[0013] The PFC-PWM controller includes a the sequencer for generating a first enable-signal and a second enable-signal. The first and second enable-signals are used to enable or disable the PFC signal and the PWM signal. Whenever the line input voltage exceeds a third threshold, this indicates a no-brownout condition. A first-state is created if the no-brownout condition sustains longer than a second delay-time. The first-state and an enabled ON/OFF signal achieve a second-state. A third-state is created if the second-state sustains longer than a third delay-time. The third-state will enable the first enable-signal when the burst-signal is disabled. Once the first feedback voltage is higher than a fourth threshold, this indicates a PFC-ready condition, in which the PFC-ready condition associates with the third-state that enable a fourth-state. When the fourth-state sustains longer than a fourth delay-time, this creates a fifth-state. The fifth-state enables the second enable-signal.

[0014] The sequencer generates a proper sequence to switch the PFC signal and the PWM signal. This protects the power converter from incorrectly operating. The

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pulse width of the pulse-signal ensures a dead time to be inserted after the PFC signal is turned off and before the PWM signal is turned on. This dead time spreads ~~the~~ switching signal, such as the PWM signal and the PFC signal, and reduces ~~the~~ switching noise. Furthermore, the pulse width of the pulse-signal is increased and ~~the~~ a frequency of the pulse-signal is decreased in response to ~~the decrease~~ a decrement of the discharge current. Thus, ~~the~~ power consumption of the power converter under light-load and zero-load conditions can be effectively reduced.

[0015] It is to be understood that both the foregoing general descriptions and the following detailed descriptions are exemplary, and are intended to provide further explanation of the invention as claimed.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0017] FIG. 1 shows a block diagram of a power converter including a PFC-PWM controller according to the present invention.

[0018] FIG. 2 shows a preferred embodiment of a power manager of the PFC-PWM controller according to the present invention.

[0019] FIG. 3 shows a preferred embodiment of an oscillator of the PFC-PWM controller according to the present invention.

[0020] FIG. 4 is a timing diagram showing the signal waveforms of the oscillator of the PFC-PWM controller according to the present invention.

[0021] FIG. 5 shows a preferred embodiment of a sequencer of the PFC-PWM

controller according to the present invention.

[0022] FIG. 6 shows a preferred embodiment of a delay timer according to the present invention.

[0023] FIG. 7 shows a preferred embodiment of a PFC stage of the PFC-PWM controller according to the present invention.

[0024] FIG. 8 shows a preferred embodiment of a PWM stage of the PFC-PWM controller according to the present invention.

[0025] FIG. 9 is a timing diagram showing the signal waveforms of the PFC stage and the PWM stage of the PFC-PWM controller according to the present invention.

DESCRIPTION OF THE P̶R̶E̶F̶E̶R̶R̶E̶D̶ EMBODIMENTS

[0026] FIG. 1 shows t̶h̶e̶ a block diagram of a power converter 5 including a PFC-PWM controller 200 according to the present invention. The PFC-PWM controller 200 includes a PFC stage 10. The PFC stage 10 generates a PFC signal OP1 in response to t̶h̶e̶ a line voltage $V_{IN}$ and a feedback voltage PFC_FB to control the s̶w̶i̶t̶c̶h̶e̶s̶ ̶o̶f̶ ̶a̶ PFC boost converter 20 (̶n̶o̶t̶ ̶s̶h̶o̶w̶n̶)̶. The feedback voltage PFC_FB is derived from t̶h̶e̶ a PFC boost converter feedback loop 43. When the feedback voltage PFC_FB decreases, this represents a proportional d̶e̶c̶r̶e̶a̶s̶e̶ decrement of t̶h̶e̶ a load 86 of the power converter 5, and an i̶n̶c̶r̶e̶a̶s̶e̶ increment in t̶h̶e̶ an output voltage $V_{O1}$ of the PFC boost converter 20.

[0027] The PFC-PWM controller 200 further includes a PWM stage 30 for generating a PWM signal OP2 in response to a feedback voltage PWM_FB. The PWM signal OP2 is used to control t̶h̶e̶ ̶s̶w̶i̶t̶c̶h̶e̶s̶ ̶o̶f̶ a DC-to-DC power converter 40 (̶n̶o̶t̶ s̶h̶o̶w̶n̶)̶. The feedback voltage PWM_FB is derived from t̶h̶e̶ a DC-to-DC power converter feedback loop 46. When the feedback voltage PWM_FB decreases, this

represents a proportional ~~decrease~~ decrement of the load 86 of the power converter 5,

and an ~~increase~~ increment in ~~the~~ an output voltage $V_{O2}$ of the DC-to-DC power

converter 40.

[0028] FIG. 2 shows a power manager 50 of the PFC-PWM controller 200

according to the present invention. The power manager 50 generates a discharge current

$I_D$ and a burst-signal BST. When ~~the~~ a magnitude of the feedback voltage PFC_FB

drops below ~~the~~ a magnitude of a first green-threshold voltage $V_{RA}$, the discharge

current $I_D$ will be reduced, so that it is proportional ~~with~~ to the feedback voltage

PFC_FB. When ~~the~~ a magnitude of the feedback voltage PWM_FB drops below ~~the~~ a

magnitude of a second green-threshold voltage $V_{RB}$, the discharge current $I_D$ will be

reduced, so that it is also proportional to the feedback voltage PWM_FB. Thus, ~~the~~ a

magnitude of the discharge current $I_D$ will decrease whenever the feedback voltage

PWM_FB or the feedback voltage PFC_FB decreases below certain levels.

[0029] The burst-signal BST is used to disable the PFC signal OP1 under a

suspended condition for power saving. When the boost-signal BST becomes logic-high,

the PFC signal OP1 will be logic-low, thereby disabling the operation of the PFC boost

converter 20. As FIG. 2 shows, to generate the burst-signal BST, the discharge current

$I_D$ mirrors a green-current $I_G$. ~~The~~ A magnitude of the green-current $I_G$ will be

proportional to the discharge current $I_D$. The green-current $I_G$ will be converted to a

green-voltage $V_G$ to be compared with a threshold voltage $V_{R1}$ in a comparator 63.

When ~~the~~ a magnitude of the green-voltage $V_G$ decreases below ~~the~~ a magnitude of a

the threshold voltage $V_{R1}$, the PFC-PWM controller 200 will enter a low-load state.

When the duration of the low-load state exceeds a first delay-time, the PFC-PWM

controller will enter the suspended condition. The burst-signal BST will be logic-low

when the feedback voltage PFC_FB exceeds a threshold voltage $V_{R2}$, while the

PFC-PWM controller 200 is under the suspended condition.

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[0030] FIG. 3 shows an oscillator 90 of the PFC-PWM controller 200 according to the present invention. The oscillator 90 generates a ramp-signal RMP, a slope-signal SLP and a pulse-signal PLS. The ramp-signal RMP and the slope-signal SLP are synchronized with the pulse-signal PLS. The PFC signal OP1 is generated from comparing the feedback voltage PFC_FB and the slope-signal SLP. The PWM signal OP2 is generated from comparing the feedback voltage PWM_FB and the ramp-signal RMP. The rising-edge of the pulse-signal PLS disables the PFC signal OP1. The falling-edge of the pulse-signal PLS enables the PWM signal OP2. Therefore the pulse-signal PLS is inserted in between the PFC signal OP1 and the PWM signal OP2 to avoid simultaneous on/off switching.

[0031] ~~The~~ A pulse width of the pulse-signal PLS will increase in response to ~~the~~ ~~decrease~~ a decrement in the discharge current $I_D$. Therefore, the frequency of the pulse-signal PLS is decreased under light-load and zero-load conditions. As the frequency of the pulse-signal PLS decreases, the switching frequency of the PFC signal OP1 and the PWM signal OP2 will also be reduced. Thus, the power consumption of the power converter can be reduced under light-load and zero-load conditions.

[0032] FIG. 5 shows a sequencer 70 of the PFC-PWM controller 200 according to the present invention. An ON/OFF signal is used to turn on the power converter 5. The sequencer 70 will generate an enable-signal PFC_EN to control the PFC signal OP1 and generates an enable-signal PWM_EN to control the PWM signal OP2.

[0033] When the line input voltage $V_{IN}$ exceeds a threshold voltage $V_{R3}$, this indicates a no-brownout condition. If the no-brownout condition is sustained longer than a second delay-time, the PFC-PWM controller 200 enters a first state. If the ON/OFF signal is enabled in the first state, the PFC-PWM controller 200 will enter a second state. When the second state is sustained longer than a third delay-time, the PFC-PWM controller 200 will enter a third state. If the burst-signal BST is disabled in

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the third state, the enable signal **PFC_EN** will be enabled. A PFC-ready condition exists whenever the feedback voltage **PFC_FB** exceeds a threshold voltage $V_{R4}$. If the PFC-ready condition exists in the third state, the PFC-PWM controller **200** will enter a fourth state. If the fourth state is sustained longer than a fourth delay-time, the PFC-PWM controller **200** will enter a fifth state. When the fifth state is active, the enable signal **PWM_EN** will be enabled.

[0034] The sequencer **70** protects the power converter **5** from incorrectly operating by generating a proper sequence to control the PFC signal **OP1** and the PWM signal **OP2**. The pulse width of the pulse-signal **PLS** ensures a dead time $\underline{T_D}$, which exists after the PFC signal **OP1** is turned off and before the PWM signal **OP2** is turned on. This dead time $\underline{T_D}$ spreads ~~the~~ switching ~~signal~~ signals, such as the PFC signal **OP1** and the PWM signal **OP2**, and reduces ~~the~~ switching noise. Furthermore, the pulse width of the pulse-signal **PLS** determines the maximum duty cycle of the PFC signal **OP1** and the PWM signal **OP2**. The pulse width of the pulse-signal **PLS** is increased and the frequency of the pulse-signal **PLS** is decreased in response to the ~~decrease~~ decrement of the discharge current $I_D$. Therefore, the power consumption of the power converter **5** can be reduced under light-load and zero-load conditions.

[0035] Further referring to FIG. **2**, the power manager **50** includes a current source **60** supplied with a voltage source $V_{CC}$ for limiting ~~the~~ a maximum magnitude of the discharge current $I_D$. The power manager **50** also includes a first V-I converter, consisting of an ~~operation~~ operational amplifier **61**, a transistor **51**, and a resistor $R_A$. When the magnitude of the feedback voltage **PFC_FB** exceeds the magnitude of ~~a~~ ~~threshold voltage~~ the first green-threshold voltage $V_{RA}$, the first V-I converter will generate a first V-I current in response to the feedback voltage **PFC_FB**. ~~The~~ A magnitude of the first V-I current also depends on the resistance of the resistor $R_A$. The power manager **50** also includes a second V-I converter, consisting of an ~~operation~~

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operational amplifier **62**, a transistor **52**, and a resistor $R_B$. When the magnitude of the feedback voltage **PWM_FB** exceeds the magnitude of a threshold the second green-threshold voltage $V_{RB}$, the second V-I converter will generate a second V-I current in response to the feedback voltage **PWM_FB**. The A magnitude of the second V-I current also depends on the resistance of the resistor $R_B$.

[0036] The power manager **50** also includes a first current mirror, consisting of three transistors **53**, **55** and **57**. A source of each of the transistors **53**, **55** and **57** are connected to the current source **60**. The gates of these three transistors **53**, **55** and **57** are connected to a drain of the transistor **53**. The first V-I current flowing via the drain of the transistor **53** drives the transistor **55** to produce a first discharge current $I_1$. The first V-I current flowing via the drain of the transistor **53** also drives the transistor **57** to produce a first green-current $I_{G1}$.

[0037] The power manager **50** also includes a second current mirror, consisting of three transistors **54**, **56** and **58**. A source of each of the transistors **54**, **56** and **58** are connected to the current source **60**. A gate of each of the transistors **54**, **56** and **58** are connected to a drain of the transistor **54**. The second V-I current flowing through the drain of the transistor **54** drives the transistor **56** to produce a second discharge current $I_2$. The second V-I current flowing through the drain of the transistor **54** also drives the transistor **58** to produce a second green-current $I_{G2}$.

[0038] The first discharge current $I_1$ and the second discharge current $I_2$ are coupled together to produce the discharge current $I_D$. The first green-threshold voltage $V_{RA}$ represents the a light-load threshold for the PFC boost converter **20**. The second green-threshold voltage $V_{RB}$ represents the a light-load threshold for the DC-to-DC power converter **40**. When the feedback voltage **PFC_FB** exceeds the first green-threshold voltage $V_{RA}$, the first discharge current $I_1$ will increase accordingly. When the feedback voltage **PWM_FB** exceeds the second green-threshold voltage $V_{RB}$,

the second discharge current $I_2$ will increase accordingly.

[0039] The first green-current $I_{G1}$ and the second green-current $I_{G2}$ are coupled together to produce the green-current $I_G$. The green-current $I_G$ is converted to a green-voltage $V_G$ via a resistor $R_C$. The resistor $R_C$ is connected between a drain of the transistor 57 and the a ground reference. The green-voltage $V_G$ is compared with the threshold voltage $V_{R1}$ in a the comparator 63. A positive input of the comparator 63 is supplied with the threshold voltage $V_{R1}$. A negative input of the comparator 63 is connected to the resistor $R_C$.

[0040] The power manager 50 also includes a first delay-timer 65. The first delay-timer 65 determines the first delay-time. An input of the first delay-timer 65 is connected to an output of the comparator 63. A hysteresis comparator 69 is used to compare the feedback voltage PFC_FB with a threshold voltage $V_{R2}$. A negative input of the hysteresis comparator 69 is supplied with the feedback voltage PFC_FB. A positive input of the comparator 69 is supplied with the threshold voltage $V_{R2}$. An output of an AND gate 67 produces the burst-signal BST. An output of the first delay-timer 65 and an output of the comparator 69 are respectively connected to a first input and a second input of the AND gate 67. The burst-signal BST will become logic-low when the magnitude of the feedback voltage PFC_FB exceeds the a magnitude of the threshold voltage $V_{R2}$. The burst-signal BST will be disabled when the feedback voltage PFC_FB is higher than the threshold voltage $V_{R2}$, which ensures that the an output of the DC-to-DC power converter 40 can be well regulated. If the magnitude of the feedback voltage PFC_FB decreases below the magnitude of the threshold voltage $V_{R2}$, the PFC boost converter 20 will be unable to supply sufficient output voltage $V_{O1}$ to the DC-to-DC power converter 40. Therefore, the PFC boost converter 20 is not allowed to turn off for power saving.

[0041] Further referring to FIG. 3, the oscillator 90 includes a current source 100

for supplying ~~the~~ a ramp-charge current of the ramp-signal **RMP** and ~~the~~ a

slope-discharge current of the slope-signal **SLP**. The oscillator **90** also includes a ~~first~~

third current mirror consisting of three transistors **120, 121** and **122**. A source of each of

the transistors **120, 121** and **122** are connected to the ground reference. A gate of each

of the transistors **120, 121** and **122** are connected to a drain of the transistor **120**. The

current source **100** drives the drain of the transistor **120** to produce ~~a~~ the slope-discharge

current via a drain of the transistor **121**. The current source **100** also drives the drain of

the transistor **120** to produce an osc-current via a drain of the transistor **122**.

[0042] Two switches **105** and **106,** and a capacitor **99** are used to generate the

slope-signal **SLP**. The two switches **105** and **106** are controlled to alternately conduct.

The two switches **105** and **106** are connected in series. A reference voltage $V_H$ is

supplied to a first terminal of the switch **105**. A second terminal of the switch **106** is

connected to the drain of the transistor **121**. The capacitor **99** is coupled to ~~the~~ a junction

of the switch **105** and the switch **106**. Once the switch **105** is turned on, the capacitor **99**

will be charged up to the reference voltage $V_H$.

[0043] The slope-discharge current discharges the capacitor **99** when the switch

**106** is turned on. The two transistors **124** and **125** are connected to form a ~~second~~ fourth

current mirror. The sources of two transistors **124** and **125** are both supplied with the

voltage source $V_{CC}$. The gates of two transistors **124** and **125** are connected to a drain of

the transistor **124**. The osc-current drives the drain of the transistor **124** to produce ~~a~~ the

ramp-charge current via a drain of the transistor **125**. Two transistors **128** and **129** are

connected to form a ~~third~~ fifth current mirror. The sources of two transistors **128** and

**129** are connected to the ground reference. The gates of the two transistors **128** and **129**

are connected to a drain of the transistor **128**. The discharge current $I_D$ drives the drain

of the transistor **128** to produce a ramp-discharge current via a drain of the transistor

**129**.

[0044] Two switches 101 and 102, and a capacitor 97 are used to produce the ramp-signal RMP. The switches 101 and 102 are controlled to alternately conduct. The two switches 101 and 102 are connected in series. The ramp-charge current is supplied to a first terminal of the switch 101. A second terminal of the switch 102 is ~~supplied~~ driven with the ramp-discharge current. The capacitor 97 is connected to ~~the~~ a junction of the switch 101 and the switch 102. Once the switch 101 is turned on, the ramp-charge current will start to charge up the capacitor 97. When the switch 102 is turned on, the ramp-discharge current will discharge the capacitor 97. The negative inputs of a comparator 91 and a comparator 92 are connected to the junction of the switch 101 and the switch 102. This allows the ramp-signal RMP to be detected. A positive input of the comparator 91 is supplied with the reference voltage $V_H$. A positive input of the comparator 92 is supplied with a reference voltage $V_L$. The magnitude of the reference voltage signal $V_H$ is higher than the magnitude of the reference voltage $V_L$.

[0045] A NAND gate 93 and a NAND gate 94 are used for generating the pulse-signal PLS at an output of the NAND gate 93. The output of the NAND gate 93 is connected to a second input of the NAND gate 94. An output of the NAND gate 94 is connected to a second input of the NAND gate 93 to form a latch circuit. A first input of the NAND gate 93 is connected to an output of the comparator 91. A first input of the NAND gate 94 is connected to an output of the comparator 92. An inverter 95 is used to generate an inverse pulse-signal INV. An input of the inverter 95 is connected to the output of the NAND gate 93. The pulse-signal PLS is used to enable the switches 102 and 105. The inverse pulse-signal INV is used to enable the switches 101 and 106.

[0046] FIG. 4 shows the signal waveforms of the oscillator 90 of the PFC-PWM controller 200 of the present invention. The ramp-charge current and the capacitance of the capacitor 97 determine ~~the~~ a rising time of the ramp-signal RMP. The pulse-signal PLS becomes logic-high once the magnitude of the ramp-signal RMP reaches the

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magnitude of the reference voltage $V_H$. The amplitude of the ramp-discharge current and the capacitance of the capacitor 97 determine ~~the~~ a falling time of the ramp-signal RMP. The pulse-signal PLS will become logic-low when the ramp-signal RMP decreases to the reference voltage $V_L$. ~~The~~ A duration of the falling time of the ramp-signal RMP also determines the ~~pulse-width~~ dead time $T_D$ of the pulse-signal PLS.

[0047] The ~~pulse-width~~ dead time $T_D$ of the pulse-signal PLS increases in response to the ~~decrease~~ decrement of the discharge current $I_D$. The slope-signal SLP is maintained at ~~the~~ a level of the reference voltage $V_H$ during ~~the~~ a level of the pulse-signal PLS is logic-high. The falling time of the slope-signal SLP is generated in response to the magnitude of the slope-discharge current and the capacitance of the capacitor 99. The duration of the falling time of the slope-signal SLP is equal to the duration of the rising time of the ramp-signal RMP.

[0048] Further referring to FIG. 5, the sequencer 70 includes a comparator 75 for comparing the line input voltage $V_{IN}$ with a threshold voltage $V_{R3}$. A positive input of the comparator 75 is supplied with the line input voltage $V_{IN}$. A negative input of the comparator 75 is supplied with the threshold voltage $V_{R3}$. When the line input voltage $V_{IN}$ is sufficiently high, this indicates ~~a~~ the no-brownout condition. A second delay-timer 71 is used to determine a second delay-time. An input of the second delay-timer 71 is connected to an output of the comparator 75. Once the no-brownout condition is sustained longer than the second delay-time, the sequencer 70 will enter a first state.

[0049] The sequencer 70 also includes an AND gate 77. A first input of an AND gate 77 is connected to an output of the second delay-timer 71. A second input of the AND gate 77 is supplied with the ON/OFF signal. When the signal supplied by an output of the AND gate 77 is high, the sequencer 70 will enter a second state.

[0050] A third delay-timer **72** is used to determine a third delay-time. When the second state is sustained longer than the third delay-time, the sequencer **70** will enter a third state. An input of the third delay-timer **72** is connected to the output of the AND gate **77**. An input of an inverter **74** is supplied with the burst-signal **BST**. An AND gate **79** is used to produce the enable-signal **PFC_EN**. A first input of the AND gate **79** is connected to an output of the inverter **74**. A second input of the AND gate **79** is connected to an output of the third delay-timer **72**. A comparator **76** is used for comparing the feedback voltage **PFC_FB** with a threshold voltage $V_{R4}$. A positive input of the comparator **76** is supplied with the feedback voltage **PFC_FB**. A negative input of comparator **76** is supplied with the threshold voltage $V_{R4}$. When an output signal of the comparator **76** is logic-high, this indicates that the sequencer **70** is in a PFC-ready state.

[0051] The sequencer **70** also includes an AND gate **78**. A first input of the AND gate **78** is connected to the output of the third delay-timer **72**. A second input of the AND gate **78** is connected to an output of the comparator **76**. When the signal supplied by an output of the AND gate **78** becomes logic-high, then the sequencer **70** will enter a fourth state. A fourth delay-timer **73** determines a fourth delay-time. An input of the fourth delay-timer **73** is connected to the output of the AND gate **78**. If the fourth state is sustained longer than the fourth delay-time, the sequencer **70** will enter a fifth state. When the sequencer **70** is in the fifth state, the enable-signal **PWM_EN** will be enabled.

[0052] FIG. 6 shows a preferred embodiment of constructing a delay-timer. The preferred embodiment of the delay timer according to the present invention is built from five cascaded flip-flops. It includes five flip-flops **81, 82, 83, 84** and **85**. It is to be understood that the present invention also covers variations to this delay-timer. The delay-timer may consist of any number of cascaded flip-flops. It is also to be understood

that the present invention also covers variations to this delay-timer, wherein entirely different means are used to produce a delay-time. The purpose here is simply to demonstrate one possible implementation of a delay-timer. The operation of this circuit will be well known to those skilled in the art, and therefore details thereof will not be discussed herein.

[0053] FIG. 7 shows a preferred embodiment of the PFC stage 10. A comparator 15 is used for comparing the feedback voltage **PFC_FB** with the slope-signal **SLP**. A positive input of the comparator 15 is supplied with the feedback voltage **PFC_FB**. A negative input of the comparator 15 is supplied with the slope-signal **SLP**. An input of an inverter 21 is supplied with the pulse-signal **PLS**. An input of an inverter 29 is supplied with a protection-signal **OVR1**. The protection-signal **OVR1** indicates the presence of fault conditions in the PFC boost converter 20, such as over-voltage, over-current, and over-temperature. A first input of an AND gate 26 is connected to an output of the inverter 21. A second input of the AND gate 26 is connected to an output of the inverter 29. A flip-flop 11 and a flip-flop 12 are used for producing the PFC signal **OP1** from an output of the flip-flop 12. The D-inputs of the flip-flop 11 and 12 are both supplied with the enable-signal **PFC_EN**. A clock-input of the flip-flop 12 is connected to an output of the flip-flop 11. A reset-input of the flip-flop 11 is connected to the output of the inverter 21. A reset-input of the flip-flop 12 is connected to an output of the AND gate 26. A delay circuit 17, consisting of two NOT gates 22 and 23 connected in series, has an input connected to the output of the inverter 21. A first input of an AND gate 25 is connected to an output of the comparator 15. A second input of an AND gate 25 is connected to an output of the delay circuit 17. An output of the AND gate 25 is connected to a clock-input of the flip-flop 11.

[0054] FIG. 8 shows a preferred embodiment of the PWM stage 30. A comparator 35 is used for comparing the feedback voltage **PWM_FB** with the ramp-signal **RMP**. A

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positive input of the comparator 35 is supplied with the feedback voltage PWM_FB. A negative input of the comparator 35 is supplied with the ramp-signal RMP. An input of an inverter 39 is supplied with the pulse-signal PLS. An input of an inverter 38 is supplied with a protection-signal OVR2. The protection-signal OVR2 is utilized to indicate fault conditions in the DC-to-DC power converter 40, such as over-voltage, over-current and over-temperature. A first input of an AND gate 34 is connected to an output of the comparator 35. A second input of an AND gate 34 is connected to an output of the inverter 38. The D-inputs of a flip-flop 31 and a flip-flop 32 are both supplied with the enable-signal PWM_EN. The clock-inputs of the flip-flops 31 and 32 are connected to an output of the inverter 39. A reset-input of the flip-flop 31 is connected to an output of the AND gate 34. A comparator 36 is used for comparing a threshold voltage $V_{R5}$ with the ramp-signal RMP. The comparator 36 also determines the a maximum duty cycle of the PWM signal OP2. A positive input of the comparator 36 is supplied with the threshold voltage $V_{R5}$. A negative input of the comparator 36 is supplied with the ramp-signal RMP. The output of the comparator 36 is connected to a reset-input of the flip-flop 32. An AND gate 33 generates the PWM signal OP2. A first input of the AND gate 33 is connected to an output of the flip-flop 31. A second input of the AND gate 33 is connected to an output of the flip-flop 32. A third input of the AND gate 33 is connected to the output of the inverter 39.

[0055] FIG. 9 is a timing diagram showing the waveforms of the PFC signal OP1, the PWM signal OP2, the ramp-signal RMP, and the slope-signal SLP. The PWM signal OP2 is high whenever the magnitude of the feedback signal PWM_FB exceeds the magnitude of the ramp-signal RMP. The PFC signal OP1 is high whenever the magnitude of the feedback signal PFC_FB exceeds the magnitude of the slope-signal SLP. The duration of the period dead time $T_D$ is equal to the pulse width of the pulse-signal PLS. During this period the dead time $T_D$, both the PFC signal OP1 and

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the PWM signal **OP2** are turned off.

[0056] Under light-load and zero-load conditions, the ~~length of the period~~ dead time $T_D$ will increase in response to the ~~decreases~~ decrement in the load 86 of the power converter 5. Therefore, the switching frequency and the power consumption of the power converter can be effectively reduced.

[0057] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the present invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided that they fall within the scope of the following claims and their equivalents.

ABSTRACT OF THE DISCLOSURE

The present invention discloses a PFC-PWM controller having interleaved switching. A PFC stage ~~is used to generate~~ generates a PFC signal for switching ~~the~~ a PFC boost converter ~~switches~~ of a power converter. A PWM stage ~~is used to generate~~ generates a PWM signal for switching ~~the~~ a DC-to-DC ~~power~~ converter ~~switches~~ of the power converter. The PFC-PWM controller includes a power manager for generating a discharge current and a burst-signal. Under light-load conditions, the discharge current ~~is decreased~~ decreases in proportion to ~~the~~ a load of the power converter. The burst signal is utilized to disable the PFC signal in a suspended condition for power saving. ~~The PFC-PWM controller also includes an oscillator for producing a pulse-signal, a ramp-signal, and a slope-signal. These three signals are used to correctly generate the PFC-signal and the PWM signal.~~ ~~The~~ A pulse width of the pulse-signal ensures a dead time ~~after the PFC-signal is turned off and before the PWM-signal is turned on. This dead time~~ to ~~spreads~~ spread the switching ~~signal~~ signals, such as the PFC and PWM signals, and reduces ~~the~~ switching noise. When the discharge current decreases, the pulse width of the pulse-signal will increase and ~~the~~ a frequency of the pulse-signal will decrease correspondingly. This further reduces power consumption under light-load and zero-load conditions.